Toward Atom-Scale Silicon Electronics

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Abstract

The most fundamental obstacle to continued scaling of conventional electronic devices today is random impurity doping. Here we discuss an approach in which dopants are first eliminated entirely from an otherwise standard MOSFET structure to reach ~25nm channel length and ~100nm overall dimension, providing an improved electrical interface to the atomic world. Meanwhile, STM/e-beam lithography is being extended to reach atomic resolution in selective placement of self-ordered dopant precursor molecules onto a hydrogen-terminated silicon surface. Successful epitaxial encapsulation of these ordered dopant patterns into Si and SiGe heterolayers might then provide a practical basis for true atom-scale electronics.

1. Introduction

Atom-scale electronics is an attractive concept, but enormous effort will be required even to demonstrate it in the laboratory. The recent invention of the scanning tunneling microscope (STM) has provided a means to eventually achieve this goal, but many different routes are possible and the suitability of such methods to future industrial production remains in doubt. The technique we are pursuing is based upon coating UHV-clean Si(100)-2x1 surfaces with a single monolayer of hydrogen-atom 'resist', then using the STM as a source of low-energy electrons to remove the hydrogen and expose bare silicon dangling bonds. Much has now been learned about the specific mechanisms of hydrogen desorption under these conditions, and atomic resolution can be obtained by operating in the tunneling regime at sample voltages below ~4 V where the electron beam is tightly confined [1].

Figure 1 shows our first attempt to pattern a metal on the atomic scale [2]. Hydrogen was selectively desorbed along a series of five lines ~20 Å (three dimer rows) in width spaced 60 Å apart. Two outer 100 Å-wide lines were also defined by superposition. Aluminum was then evaporated at 0.1 ML coverage onto this patterned sample at room temperature, and subsequent analysis of STM images shows that most Al adatoms have diffused over distances of ~5 nm across the (darker) H-terminated surface to be selectively captured by exposed areas of bare silicon within finer portions of this pattern. Al clusters also form on the H-terminated surface, and these appear to be nucleated by collisions between two mobile Al adatoms.

This direct evaporation technique may eventually yield an individual 'single-atom wire' by employing reduced deposition rates under optimum conditions for adatom diffusion [3]. Adapting STM exposure of H-

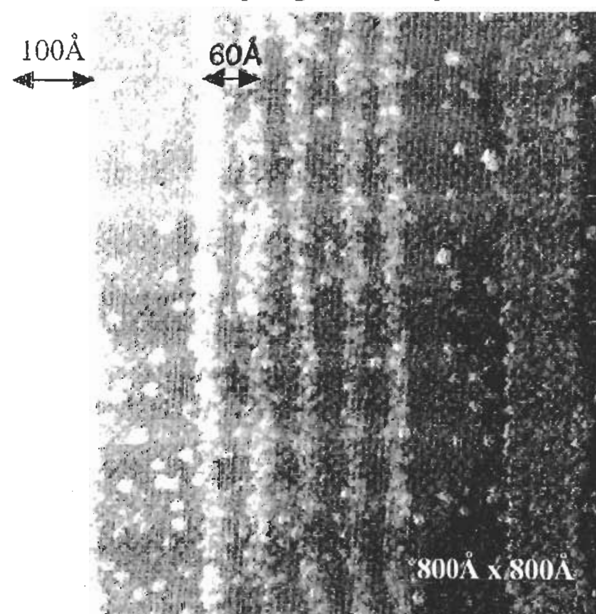


Fig.1 UHV-STM image of ~20Å-wide and 100Å-wide lines written in hydrogen termination on Si(100)-2x1:H, following deposition of 0.1ML Al at room temperature. Most metal adatoms landing within finer portions of this pattern have diffused across average distances of ~5nm on the hydrogen termination to be selectively captured by STM-exposed regions of bare silicon [2].

atom 'resist' to fabricate practical electronic circuits, however, will require a distinctly different approach which incorporates the following improvements: (1) total selectivity for bare vs. H-terminated silicon, (2) a self-stopping, self-ordered deposition reaction which avoids clusters and gaps within atom-scale patterns, and (3) passivation of the completed structure to eliminate surface states and other sources of electrical non-uniformity. Epitaxial encapsulation of selectively patterned donors and acceptors into the silicon lattice offers the ultimate level of passivation required for atom-scale devices, and a process of this type might also solve difficult problems of random impurity doping in conventional device structures.

2. Schottky Barrier Tunneling Transistors

The problem of overcoming limitations imposed by random impurity doping lies at the heart of all future progress in integrated circuit technology. At sub-100 nm channel lengths, threshold fluctuations due to varying positions of individual dopants beneath the gate is expected to be a difficult, and ultimately insurmountable, obstacle to scaling of metal-oxide-semiconductor field effect transistors (MOSFETs). Dopants can be eliminated entirely, however, by substitution of a metal silicide for heavily doped silicon in the source/drain regions. The natural Schottky barrier formed at the source and drain confines carriers in the 'off' state, and gate-induced electric fields render the source barrier nearly transparent by tunneling when the device is

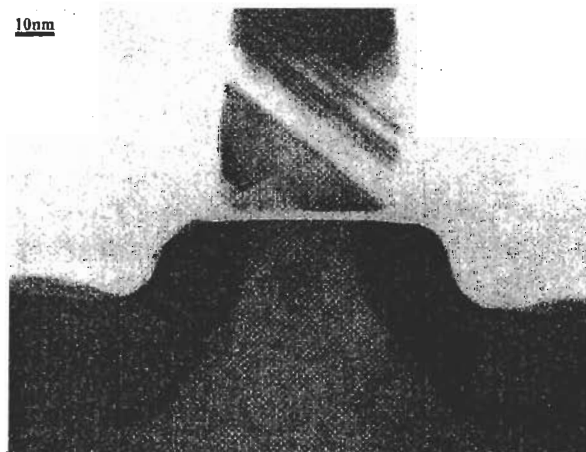


Fig.2 Cross sectional TEM image of PtSi source/drain p-MOSFET with 27 nm channel length and 19 Å gate oxide fabricated on an undoped silicon substrate [4].

turned 'on'. PtSi devices employing a low ~0.2 eV hole barrier have recently been demonstrated at ~25 nm channel length and ~100 nm overall size, as shown in Fig.2 [4]. At supply voltages of ~1.0 V with 19 Å gate oxide, current drives are ~200-300 μA/μm similar to conventional p-MOSFETs. Thermal emission limits on/off current ratio to ~25-50 at room temperature, but ratios of $\sim 10^7$ are measured at 77K. At room temperature, on/off ratios of $\sim 10^3$ can be achieved by inserting fully-depleted dopants beneath the active region. Complementary n-type SB-MOSFETs can be realized using the low n-barrier of $ErSi_2$, and a large-scale prototype on SOI has recently been reported [5]. Extraordinary scaling, reduced parasitics, and greatly simplified fabrication make these devices attractive candidates for future nanoscale CMOS. The channel length in Fig. 2 is only ~100 atomic diameters, so these extremely small MOSFETs should provide better coupling to future atom-scale devices.

3. Atom Resolved Selective Planar Doping

Long-term progress will ultimately depend upon the ability to define atom-scale conducting pathways in silicon. The basis for our approach here is self-assembly of atomically-ordered donor and acceptor arrays onto bare silicon dangling bonds exposed by STM lithography. Uniform coverages on Si(100)-2x1 are easily obtained with a number of gaseous precursors such as PH_3, AsH_3, and B_2H_6 containing the desired adatom plus hydrogen. A fractional monolayer is typically adsorbed at room temperature on clean silicon until all available dangling bonds are saturated, blocking any further reaction. No adsorption occurs on H-terminated surfaces, and substrates must be heated above ~500°C to desorb hydrogen and create new bare dangling bonds in order to sustain CVD reactions involving such molecules. For our purposes, the salient features are uniform, self-limited deposition onto bare silicon at room temperature with total selectivity to hydrogen termination.

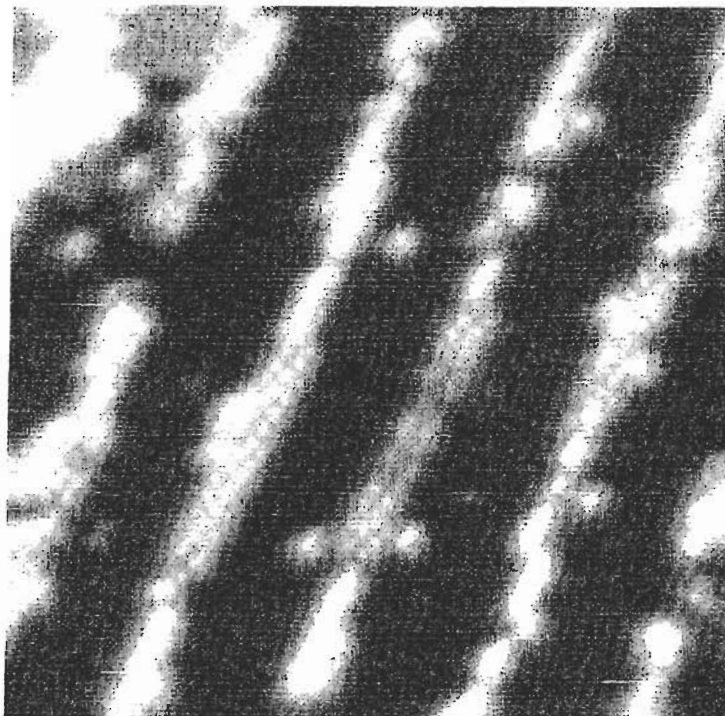
A good example may be seen in the recent UHV-STM study of PH_3 adsorption on Si(100)-2x1 reported by Wang, Bronikowski, and Hamers [6]. Molecular PH_3 is adsorbed at room temperature with strong ordering onto alternate dimers within a single row. Individual PH_3 molecules are chemisorbed in an 'on top' configuration by formation of two

P-Si bonds to the underlying Si=Si dimer, as illustrated in Fig. 3(b), breaking the weak π-bond but leaving the dimer σ-bond intact. Chemically, the P-atom assumes a pentavalent state as a result of two additional bonds to the silicon dimer through admixture of low-lying d-levels. Linear self-ordering of PH_3 molecules could presumably be used to fabricate a uniform P-atom wire along STM-exposed dimer rows of a hydrogen passivated surface similar to those in Fig. 3(a), with no adsorption occurring on the unexposed H-termination. On extended areas of bare Si(100)-2x1, PH_3 molecules form ~1/4 ML c(4x2) structures at saturation coverage with alternating adsorption sites staggered on adjacent rows.

STM lithography has already demonstrated an ability to desorb individual hydrogen atoms from particular silicon dangling bonds, so that it should be possible (though time consuming) to place PH_3 molecules onto a Si(100)-2x1:H surface in any desired 1-D or 2-D configuration, at least over small areas. The key step needed in order to transform such patterns into fully passivated, atom-scale electronic circuits is epitaxial incorporation of the individual donors into the silicon lattice without significant redistribution. Low-temperature Si UHV-CVD has demonstrated an ability to suppress vertical redistribution of B atoms to a level which is undetectable by cross sectional TEM[7]. While this is encouraging, new techniques will likely be needed in order to deposit the first few monolayers of silicon without causing redistribution of ~1/4 ML self-ordered dopant patterns, and we are now beginning experiments in this direction. Here, the STM's remarkable imaging capabilities offer a crucial advantage in following the process of dopant incorporation on the atomic scale. STM cross sectional imaging of III-V heterolayers has consistently permitted us to observe individual Si donors in GaAs to a depth of 5-6 ML below the surface. In δ-doped crystals, vertical redistribution is confined to ~2.5 Å in this system. We anticipate that dopant incorporation into Si can be followed to a similar depth during overgrowth, providing information needed in developing processes which minimize redistribution. The degree of success achieved here will, of course, determine the feasibility of atom-scale circuits using this approach.

4. Atom Scale Electronic Devices

New opportunities to control electron transport should open up if the process



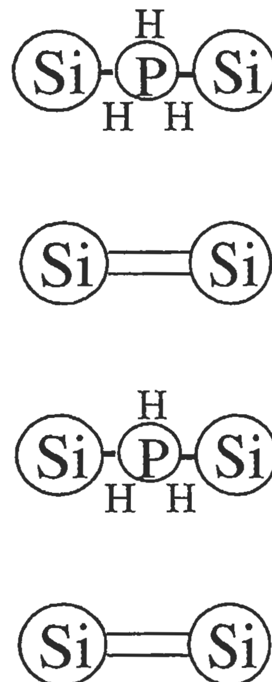


Fig.3 (a) Atom-scale lines written 30 Å apart by STM-induced desorption of hydrogen along dimer rows of an *in situ* passivated Si(100)-2x1:H surface. Brighter portions correspond to selective elimination of hydrogen atoms from either the left or right side of the silicon dimers, while thicker portions show nodal structure of the bare dimers where both hydrogen atoms are desorbed [1]. (b) Sketch of self-ordering of PH_3 molecules onto alternate dimers along a single row [after Ref. 6].

described here proves feasible. The most fundamental would be an ability to structure tunneling at the single-atom level. Tunneling depends exponentially on overlap of wavefunctions across a barrier, and two individual atoms will ordinarily be coupled only at spacings of ~5 Å or less. The hydrogenic ground state for electrons orbiting a P-atom donor in silicon, however, has a large 3-D Bohr radius $a_B \approx 2.5$ nm due to its low binding energy of ~45 meV. Electrically, each donor is therefore ~5 nm in diameter, and wavefunctions localized on different donor atoms begin to overlap at ~10 nm separation. This effect prevents carrier freezeout in randomly doped crystals at densities in excess of 10^{18} cm^{-3} (one dopant per 10 nm cube). Successful use of STM lithography to position individual dopants on a scale much finer than this immediately implies detailed control over wavefunction overlap and a means to fabricate artificial conducting lattices of any desired structure. Ordered arrays with spacing greater than ~5 nm will form a half-filled tight-binding band in which the binding energy for the highest occupied states at the Fermi level is roughly equal to that of an isolated impurity. Atom-scale circuits of this type would therefore require cooling to liquid He temperatures.

Continuously depassivated areas will adsorb a very high density, ~1.7×10^{14} cm^{-2}, of dopant precursors at saturation coverage. Nearest neighbor distances within a self-ordered PH_3 c(4x2) array are 7.7 Å along a dimer row and 8.6 Å across, much smaller than the ~5nm Bohr diameter. Simple tight-binding models can then no longer be applied. If these high density donor sheets can be overgrown and activated, electrons should be tightly confined to the lowest subbands in the growth direction by very large electric fields at average distances of ~3 Å-5 Å from the dopant plane. Lateral confinement at the edge of a patterned 2-D dopant sheet, however, will be far weaker. Initial estimates predict a characteristic length of ~4 nm for lateral decay of the bound-state wavefunctions, comparable to the single-impurity Bohr diameter. If this is indeed the case, it should eventually become possible to define lateral tunnel junctions with uniform impedance and no offset charge. Arrays of this kind might then improve the reproducibility of single-electron devices to the point where they could be considered for use in future low-power, ultra-high density integrated circuits at reduced temperatures.

At room temperature, lateral patterning of self-ordered dopant sheets on a ~10 nm scale could find important applications in structuring conventional field-effect transistors at the limits of scaling. Most proposals of this type involve dual-gates and a very thin undoped Si channel of length L~10-30 nm lying between heavily-doped source and drain. Figure 4 illustrates the 'ultimate' MOSFET structure recently analyzed by Pikus and Likharev[8] as an example. In their simulations, the channel thickness is 2 s=15 Å and channel length is L=10 nm. Source and drain are assumed to be uniformly doped at $N_D = 3 \times 10^{20}$ cm^{-3}, and only ~15 or so dopants will thus be contained within the physically important volumes of source and drain for a channel of width equal to length. At the present time, there is no way to define a ~10 nm-long channel with abrupt transitions to heavily doped source/drain. The technique described here could, if successful, make it possible to delineate such structures and grow them into SOI or Si/SiGe channels with quasi-atomic precision. The potential to both accurately control electron transport at the single-atom level and to extend the scaling of conventional transistors makes this a very interesting area for further rersearch.

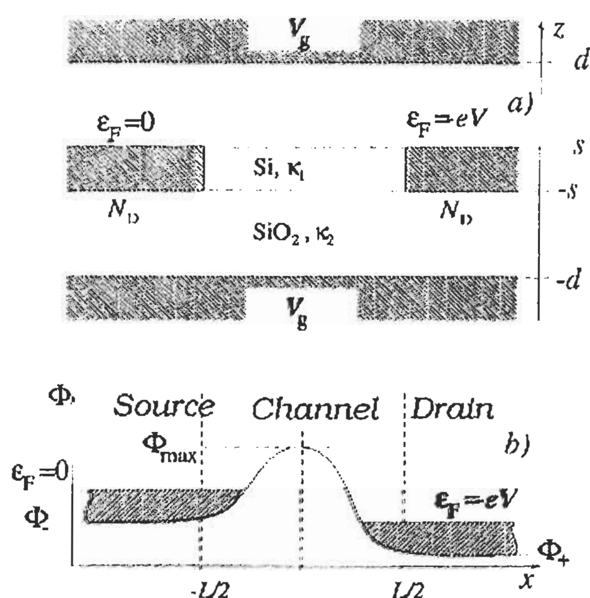


Fig.4 (a) Sketch of the MOSFET structure considered by Pikus and Likharev[8], and (b) the conduction band barrier to be modulated by a dual-gate potential.

Acknowledgements

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